Application No:
Applicant: MATSUSHITA ELECTRIC INDUSTRIAL CO., LTD.
Our ref: EP25265-07303
Date: September 17, 2002

Claims

1. A method for processing a video signal, comprising the steps of:

receiving (s2) a video signal including a plurality of subsequent video images,

superimposing (s3) an additional image on a video image of said video signal in accordance with a control signal (53) for producing a mixed video signal, said control signal (53) indicating an image area for superimposing said additional image,

processing (s4) said mixed video signal for producing a processed video signal, and

outputting (s5) said processed video signal,

characterized in that

the processing (s4) of said mixed video signal is performed in accordance with said control signal (53) by processing said mixed video signal differently for separate image areas.

2. A method for processing a video signal according to claim 1, wherein said video signal and said control signal (53) have the same pixel clock frequency.

3. A method for processing a video signal according to claim 1 or 2 further comprising the step of generating the image data of said additional image together with said control signal (53).

4. A method for processing a video signal according to claim 3 wherein said image data include user interaction information to be displayed on a screen together with the video signal.

5. A method for processing a video signal according to any of claims 1 to 4 wherein said step of processing (s4) said mixed video signal includes the step of interpolating image data of said mixed video signal.

6. A method for processing a video signal according to any of claims 1 to 5 wherein said step of processing (s4) said mixed video signal includes the step of performing a motion compensation of said mixed video signal.

7. A method for processing a video signal according to any of claims 1 to 6 wherein said processing step (s4) includes the step of de-interlacing said mixed video signal for producing a progressive video signal.

8. A method for processing a video signal according to any of claims 1 to 7 wherein said processing step (s4) converts the frame rate of said mixed video signal from a first frame rate to a second frame rate.

9. A method for processing a video signal according to claim 8 wherein said frame rate conversion employs at least one of image data interpolation, motion compensation and using the unprocessed video data for generating video images of the second frame rate.

10. A method for processing a video signal according to claim 9 wherein the employed image processing is selected in accordance with said control signal (53).

11. A method for processing a video signal according to claim 9 or 10 wherein the image data of said additional image are only used without any further processing.

12. A method for processing a video signal according to claim 9 or 10 wherein the image data of said additional image are only subjected to image data interpolation.

13. A method for processing a video signal according to claim 9 or 10 wherein the image data of said video signal surrounding said additional image in said mixed video signal are only subjected to image data interpolation.

14. A method for processing a video signal according to any of claims 1 to 13, wherein said control signal (53) further comprising processing selection information in accordance with the image content of the mixed video signal.

15. A video processing unit for receiving a video signal (50) including a plurality of subsequent video images and for outputting a processed video signal (56) comprising:

a mixer (52) for producing a mixed video signal (54) by superimposing an additional image (51) on a video image of said video signal (50) in accordance with a control signal (53), said control signal (53) indicating an image area for superimposing said additional image (51), and

a processing circuit (55) for processing said mixed video signal (54),

characterized in that

said processing circuit (55) is adapted for processing said mixed video signal (54) in accordance with said control signal (53) by processing said mixed video signal (54) differently for separate image areas.

16. A video processing unit according to claim 15, further comprising a display (67) for displaying said processed video signal (56, 66).

17. A video processing unit according to claim 15 or 16, wherein said video signal (50) and said control signal (53) have the same pixel clock frequency.

18. A video processing unit according to any of claims 15 to 17, further comprising an image generator (64) for generating said additional image (51) together with the corresponding control signal (53).

19. A video processing unit according to claim 18, wherein said image generator (64) being an on-screen-display circuit.

20. A video processing unit according to any of claims 15 to 19, wherein said processing circuit (55, 65) being adapted to interpolate image data.

21. A video processing unit according to any of claims 15 to 20, wherein said processing circuit (55, 65) being adapted to apply motion compensation.

22. A video processing unit according to any of claims 15 to 21, wherein said processing circuit (55, 65) being adapted to de-interlace said mixed video signal (54).

23. A video processing unit according to any of claims 15 to 22, wherein said processing circuit (55, 65) being a frame rate converter for converting the frame rate of said mixed video signal (54) from a first frame rate to a second frame rate.

24. A video processing unit according to any of claims 15 to 23, wherein said processing circuit (55, 65, 70) comprises different processing paths (71, 72, 73) for processing said mixed video signal (54) and a selector (74) for selecting one of said processing paths (71, 72, 73) in accordance with said control signal (53, 77, 78).

25. A video processing unit according to claim 24 wherein said processing paths (71, 72, 73) comprising at least one of image interpolation (72), motion compensation (71) and using the unprocessed video data (73).

26. A video processing unit according to claim 24 or 25 wherein said selector (74) comprises at least a binary switch (75, 76).

27. A video processing unit according to any of claims 24 to 26 wherein said selector (74) comprises a cascade of binary switches (75, 76).

28. A video processing unit according to claim 28 or 29 wherein each switch (75, 76) being controlled by a binary control signal (77, 78).

29. A video processing unit according to any of claims 15 to 28, wherein said video processing unit being one of a television receiver, a DVB receiver, a video monitor, a video recorder and a video playback device, including a DVD-player, a video-cd player and other digital video playback devices.